REMARKS

This is in response to the Office Action dated October 14, 2005. Claims 1-8 were rejected as indefinite under 35 USC 112 and claims 1-4, 6 and 7 were rejected as unpatentable under 35 U.S.C. §103. Claims 1-4, 6 and 7 are amended. Reconsideration of the claims as amended is respectfully solicited.

I. DRAWING CORRECTION

Attached is a replacement sheet of drawings containing a revised FIG. 3, revised to include the legend - Prior Art - as required.

II. SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Also attached is a supplemental Information Disclosure Statement correcting the citation of the PG-PUB document. The required fee is submitted.

III. REJECTION UNDER 35 USC 112

Claims 1-8 were rejected as indefinite under 35 USC 112 because it was not clear whether "a command from a master device" in claim 1 referred to the command recited in the "staging register" clause. In claim 1, "command" has been corrected to "information" in the "staging register" clause (which is consistent with the preamble which states that the return command register stores identification), and the "control device" clause is clarified to recite that it is responsive to a command from the master device whose identification is stored in the staging register, as well as to the identification in the staging register. Conforming amendments are made to claims 2, 3 and 6.

Claims 3-8 were rejected as indefinite under 35 USC 112 because "the first identification" in claims 3 and 6 did not have clear antecedent basis. The last clause of claims 3 and 6 is amended to recite that the next-ordered identification that was transferred to the staging register is validated, the next-ordered identification being that transferred from the return command register. Thus, the validation register contains a

representation of the validity of the identification in the staging register, and the control device is responsive to an invalid identification in the staging register to (1) "transfer the next-ordered identification from the return command register to the staging register", (2) "validate the next-ordered identification [that had been} transferred to the staging register..." and (3) "release the split of the corresponding master device". Conforming amendments are made to claims 4 and 7.

IV. REJECTION OF CLAIMS 1 AND 2 OVER ADMITTED PRIOR ART AND MARISETTI

Claims 1 and 2 were rejected as unpatentable over a combination of the admitted prior art and Marisetty (US 5,574,868). The Examiner notes that the admitted prior art does not explicitly disclose a staging register for storing a master device's identification whose command is highest in order. To meet this deficiency, the Examiner notes that Marisetty teaches a prediction technique to improve latency dealing with splits. The Examiner notes that Marisetty discloses a FIFO that stores retrieved data; the Examiner equates the data as "equivalent to the identification of a master device".

Marisetty describes a system in which latency can be decreased (in some cases) by predicting the amount of time required to acquire requested data from a memory and re-grant the system bus to the requesting master device at the appropriate time. If the time required for a particular transaction cannot be predicted, Marisetty simply reverts to his admitted prior art and stores the retrieved data in FIFO 30 and re-grants the system bus to the requesting master device upon storage.

Marisetty's master device (or agent) 12 transmits a read request to memory controller 14, which decodes the request and transmits it on to a memory 16 from where the requested data are accessed. Col. 3, lines 9-14. The split is then initiated, allowing other master devices use of system bus 10. See col. 2,

lines 3-14. Using the read request, memory controller 14 predicts the amount of time required by the memory to acquire the data onto memory bus 18, and provides an early (system) bus request signal to predictor/arbiter 22 to cause memory controller 14 to re-grant the system bus 10 to the requesting master device 12. Col. 3, lines 14-19. Predictor/arbiter 22 returns a bus grant signal to memory controller 14 to enable direct connection between buses 10 and 18 (through multiplexer 26) so that data on memory bus 18 is transferred directly to the requesting master device 12. Col. 3, lines 46-61. On the other hand, if the time for data acquisition cannot be determined, the data are simply stored in FIFO 30 for transfer through multiplexer 26 after the bus communication is re-established by memory controller 14. Col. 3, line 62 to col. 4, line 3.

Applicant reduces overall latency by allowing re-arbitration of the system bus for the next master device once the slave device commences action on the transaction for the next prior master device. While this re-arbitration might be termed an "early request," it is initiated by commencement of the transaction for the next prior master device, whereas Marisetty's "early request" is predicated on a predicted time of completing a transaction.

Importantly, Marisetty's "early request" operates to re-grant system bus use to the master device whose transaction request is being presently honored; Applicant's "early request" releases the split on the next master device following the one whose transaction request is presently being honored.

Marisetty's predictor/arbiter 22 likely includes a register that stores identifications of master devices (see col. 2, lines 11-14), arguably on a first-in, first-out basis. But Marisetty neither explicitly, nor implicitly describes

> a staging register coupled to the return command register for storing an identification of a master

> device whose identification is highest in order in the return command register,

nor

> a control device responsive to a command from the master device whose identification is stored in the staging register and to the identification in the staging register to release a split of the master device next in the return command register,

as recited in claim 1. Thus, where applicant releases the split on the next master device in the return command register upon receipt of a transaction command from the prior master device, Marisetty relies entirely on a predicted time of transaction to re-arbitrate.

The Examiner states that "the stored data [in FIFO 30] is equivalent to the identification of a master device," presumably to suggest that Marisetty's FIFO 30 is equivalent to Applicant's claimed return command register. It is respectfully submitted that the data in FIFO 30 do not identify a master device. In the context of the specification, "identification" of a master device cannot be construed as the data retrieved from memory in response to the master device's request. Thus as described at page 8, line 15 of Applicant's specification, the HMASTER code from arbiter 14 identifies the master device using the system bus and accessing the slave device.

For the reasons given, the rejection of claims 1 and 2 on the basis of the admitted prior art and Marisetty should be withdrawn.

V. REJECTION OF CLAIMS 3,4,6 AND 7 OVER ADMITTED PRIOR ART, MARISETTI AND DURDAN.

Claims 3, 4, 6 and 7 were rejected as unpatentable over the combination of the admitted prior art, Marisetty and Durdan (5,058,006). Since parent claims 1 and 2 are patentable for the reasons given above, claims 3, 4, 6 and 7 are also patentable. Moreover, it is respectfully submitted that Durdan's teachings are neither combinable with either the admitted prior art or the

teachings of the Marisetty patent, nor would any such attempted combination result in the invention of claims 3, 4, 6 or 7.

Durdan describes filtering invalidates associated with a cache memory on a private processor bus. Col. 5, lines 12-19. The Durdan system employs two-tiered cache system composed of a primary cache 20 and a backup cache 22. The primary cache includes a primary cache tag store 44, while the backup cache contains both a backup cache tag store 42 and a copy of the primary cache tag store 40 (i.e., copy of 44). During a write transaction, if the address of the write access is identified in either the backup cache tag store or the copy of the primary cache store, memory interface 24 issues an invalidate and the write transaction is completed in either the backup cache 22 or the primary cache 20, as appropriate, without involving the system bus 12. If the location is not found in either cache tag store, the write transaction is completed over the processor (system) bus 12 with a main memory 10. Col. 7, lines 39-56.

Durdan does not explicitly or inherently disclose

> a validation register containing a representation of the validity of the identification in ... [a] staging register ... [that stores an identification of a master device whose identification is highest in order in a return command register that stores identifications of split master devices on a first-in, first-out order, where a] representation that the identification in the staging register is invalid ... transfer[s] the next-ordered identification from the return command register to the staging register, ... validate[s] the next-ordered identification transferred to the staging register in the validation register and ... release[s] the split of the corresponding master device,

as recited in claims 3 and 6. Nor does Dordan explicitly or inherently disclose that

> a command from the corresponding master device ... invalidate[s] the next-ordered identification transferred to the staging register,

as recited in claims 4 and 7. Moreover, nothing in Dordan, Marisetty or the admitted prior art suggests how Dordan's

validation scheme might be applied to split transaction processing as to be modified for use in the admitted prior art or Marisetty's system.

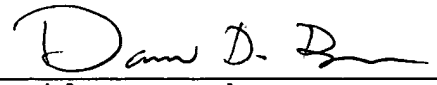
The Examiner cites Dordan's desire to avoid system saturation while preserving cache coherency. Nevertheless, it cannot be overlooked that cache coherency deals with coherency between Durdan's main memory 10 and Durdan's cache memories 20 and 22. Filtering using Durdan's technique reduces the need for cache coherency by limiting transactions to the cache and does not involve the system bus where the write address is found in a cache memory on the private bus. Applicant's validation, on the other hand, is used in allocating processors to the system bus for various transactions.

In view of the foregoing, it is respectfully submitted that claims 1-8 as amended meet the requirements of 35 USC 112, and are patentable over the admitted prior art in combination with Marisetty or in combination with both Marisetty and Dordan. Accordingly, claims 1-8 are allowable, and that action is respectfully solicited.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 12-2252.

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

By: 

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